SEMICONDUCTOR DEVICE AND ITS PRODUCTION PROCESS

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device, particularly to a semiconductor device equipped with MOS transistors.

Silicon oxide is a material having excellent insulating properties, featuring a bandgap of as large as 8.0 eV. Thanks to its high insulating performance, this material has been dominantly used for insulating films such as gate insulators and layer insulators in semiconductor devices.

In recent years, however, with miniaturization of semiconductor devices, thinning of the gate insulators has become an essential requirement, and oxide films with a thickness of less than 3.0 nm have come to be used as such insulators. Decrease of insulating film thickness to less than 3.0 nm entails an inegligibly high rise of tunneling current and power consumption.

It is known that tunneling current can be classified roughly into two types: Fowler-Nordheim tunneling current (FN current) and direct tunneling current (DT current). FN current is a current which is caused to flow as the electrons tunnel the triangular potential produced as a result of distortion of the

energy barrier by an external electric field. DT current is a current which is caused to flow by tunneling of the electrons directly through the oxide films.

It has been disclosed that ideally FN current and DT current can be defined by using the WKB (Wentzel-Kramers-Brillouin) approximation according to, for example, the equation (A1) on page 354 of IEEE TRANSACTIONS ON ELECTRON DEVICE, Vol. 46, No. 2, making use of energy barrier Φ_B between electrode and insulating film.

Rise of tunneling current by the thinning of silicon oxide gate insulators is primarily attributable to the increase of DT current. There is a concern that when various types of high-permittivity material are used for the gate insulators, the leakage current density may elevate sharply depending on the producing method of gate electrodes or gate insulators.

SUMMARY OF THE INVENTION

provide a semiconductor device equipped with MOS transistors having high-permittivity gate insulators, in which the leakage current flowing through the gate insulators is restrained.

Another object of the present invention is to provide a semiconductor device which can be driven at high speed with low power consumption.

The present invention provides a semiconductor device comprising a semiconductor substrate, gate insulators formed on said substrate, and gate electrodes formed on said gate insulators, said gate insulators which are primarily composed of titanium oxide, zirconium oxide, hafnium oxide or titanium oxide having a rutile type crystal structure, and in which compression strain is produced, and said semiconductor device equipped with MOS transistors.

The present invention also provides a semiconductor device equipped with MOS transistors having titanium oxide gate insulators disposed between the semiconductor substrate and gate electrodes, wherein the main crystal structure of said titanium oxide is anatase type, and the strain produced in the channel region of said semiconductor substrate is tensile strain.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic sectional view showing the principal part of a semiconductor device according to Example 1 of the present invention, which view was taken along the line A-A' of FIG. 2.

FIG. 2 is a top plan view of the principal part of the semiconductor device according to Example 1 of the present invention.

FIG. 3 is a schematic sectional view of the principal part of the semiconductor device according to

Example 1 of the present invention.

FIG. 4 is also a schematic sectional view of the principal part of the semiconductor device according to Example 1 of the present invention.

FIG. 5 is a graph showing strain dependence of the bandgap of rutile type titanium oxide in Example 2 of the present invention.

FIG. 6 is a graph showing strain dependence of the barrier height of rutile type titanium oxide in Example 2 of the present invention.

FIG. 7 is a graph showing strain dependence of leakage current of the rutile type titanium oxide gate insulator in Example 2 of the present invention.

FIG. 8 is a graph showing strain dependence of the bandgap of zirconium oxide in Example 2 of the present invention.

FIG. 9 is a graph showing strain dependence of the bandgap of hafnium oxide in Example 2 of the present invention.

FIG. 10 is a schematic sectional view of the principal part of the semiconductor device according to Example 3 of the present invention.

FIGS. 11A to 11D are a flow chart of the process for manufacturing the principal part of the semiconductor device shown in FIG. 10.

FIGS. 12A to 12C are another flow chart of the process for manufacturing the principal part of the semiconductor device shown in FIG. 10.

FIG. 13 is a schematic sectional view of the principal part of the semiconductor device according to Example 4 of the present invention, which view was taken along the line A-A' of FIG. 14.

FIG. 14 is a top plan view of the principal part of the semiconductor device according to Example 4 of the present invention.

FIG. 15 is a schematic sectional view showing the sectional structure of the semiconductor device according to Example 5 of the present invention.

FIG. 16 is a planar layout of the principal part of the semiconductor device according to Example 5 of the present invention.

FIG. 17 is a graph illustrating tensile strain dependence of the bandgap of titanium oxide.

FIG. 18 is a graph illustrating tensile strain dependence of the barrier height of titanium oxide.

FIG. 19 is a graph illustrating tensile strain dependence of the leakage current density of barrier height of titanium oxide.

FIGS. 20A to 20F show a flow chart for producing the semiconductor device according to Example 5 of the present invention.

FIG. 21 is a schematic sectional view showing the sectional structure of the semiconductor device according to Example 6 of the present invention.

FIG. 22 is a schematic sectional view showing

the sectional structure of the semiconductor device according to Example 7 of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The rise of tunneling current incidental to thinning of the silicon oxide gate insulators is mostly attributable to the increase of DT current. So, it is suggested to restrain the increase of DT current by thickening the gate insulators while maintaining the dielectric properties by using titanium oxide, zirconium oxide or hafnium oxide having higher permittivity than silicon oxide for the gate insulators. For example, supposing that the permittivities of titanium oxide and silicon oxide are 60 and 4.0, respectively, the titanium oxide film of 30 nm thick will have the dielectric properties equivalent to a 2 nm thick silicon oxide film. Thus, the said titanium oxide film of 30 nm thick is called to have a silicon oxide reduced thickness of 2 nm. The actual film thickness 30 nm is called physical thickness.

In use of said high-permittivity materials for the gate insulators, there has been a problem of possible exponential increase of leakage current density depending on the method of producing the gate electrodes or gate insulators.

The present inventors have pursued studies for solving the above problem and, as a result,

disclosed the mechanism that causes an exponential increase of the density of the leakage current flowing through the gate insulators depending on the method of producing the gate electrodes or gate insulators, and its countermeasure devised by the present inventors was embodied as the present invention.

This mechanism is summarized as follows. Depending on the method of forming the gate electrodes or gate insulators, the formed high-permittivity film assumes a state of tensile strain, causing a reduction of the high-permittivity film bandgap while raising the tunneling probability to increase leakage current. In order to solve these problems, the semiconductor device of the present invention, in one embodiment thereof, comprises a semiconductor substrate, gate insulators formed on this substrate and gate electrodes formed on said insulators, said gate insulators which are primarily composed of a material selected from titanium oxide, zirconium oxide and hafnium oxide and in which [illegible] (or compressive) strain is produced, and said semiconductor device [illegible] transistors.

The semiconductor device of the present invention according to another embodiment thereof comprises a semiconductor substrate, gate insulators formed on said substrate, and gate electrodes formed on said insulators, said gate insulators which are mainly composed of titanium oxide having a rutile type crystal

structure and in which compression strain is produced, and said semiconductor device equipped with MOS transistors.

The semiconductor device of the present invention according to still another embodiment thereof comprises a semiconductor substrate, gate insulators formed on said substrate and gate electrodes formed on said insulators, said gate insulators which are primarily composed of titanium oxide having a rutile type crystal structure and in which compression strain is produced, and said semiconductor device equipped with MOS transistors in which the main composing material of said gate electrodes has a greater thermal expansion coefficient than said titanium oxide.

The semiconductor device according to yet another embodiment of the present invention comprises a semiconductor substrate, gate insulators formed on said substrate and gate electrodes formed on said insulators, said gate insulators which are primarily composed of titanium oxide having a rutile type crystal structure and in which compression [illegible] and said semiconductor device equipped with MOS transistors.

In said semiconductor devices according to the present invention, each said insulator comprises a film mainly composed of silicon oxide and an overlying film composed of a material selected from titanium oxide, zirconium oxide and hafnium oxide.

The method for producing the semiconductor device according to the present invention comprises the step of forming gate insulators mainly composed of titanium oxide having a rutile type crystal structure by depositing it on one principal surface of the semiconductor substrate, and the step of forming gate electrode films on said gate insulators.

Another embodiment of the semiconductor device producing method according to the present invention comprises the step of forming gate insulators mainly composed of titanium oxide by depositing it on one principal surface of the semiconductor substrate by CVD at a temperature of 650°C or above, and the step of forming gate electrode films on said gate insulators.

In still another embodiment of the semiconductor device producing method according to the present invention, the said gate insulator forming step comprises the step of forming a film mainly composed of silicon oxide, and a step of forming on this silicon [illegible] mainly composed of an oxide material having higher permittivity than said [illegible]. Said high-permittivity oxide is mainly composed of a material selected from titanium oxide, zirconium oxide and hafnium oxide.

The semiconductor device according to yet another embodiment of the present invention comprises a semiconductor substrate and MOS transistors formed on said substrate and having gate insulators and gate

electrodes formed thereon, wherein a first MOS transistor has a gate insulator mainly composed of a material selected from titanium oxide, zirconium oxide and hafnium oxide, and a second MOS transistor has a gate insulator with a high content of silicon oxide. It is preferable that the gate insulator of the second MOS transistor is mainly composed of silicon oxide.

In said semiconductor device, said first MOS transistor may be a transistor used for the calculators or memories, and said second MOS transistor may be a transistor used for I/O.

It is preferable that each of said MOS transistors comprises a MOS transistor having a gate insulator mainly composed of silicon oxide, and a gate insulator mainly composed of a high-permittivity material having a relative dielectric constant of 16 or more.

The semiconductor device according to still another embodiment of the present invention comprises a [illegible] substrate, gate insulators formed on said substrate, and gate electrodes formed on [illegible] insulators, said gate insulators which have a multi-layer structure mainly composed of a material selected from titanium oxide, zirconium oxide and hafnium oxide and in which compression strain is produced, and said semiconductor device equipped with MOS transistors.

In the semiconductor device according to the present invention, the gate insulator is composed of

titanium oxide, zirconium oxide, hafnium oxide, tantalum oxide, or a laminate thereof, and the state of strain in the gate insulator is mostly compression strain, so that it is possible to prevent the reduction of bandgap and to thereby minimize the tunneling current.

Further, by incorporating a structure in which the leakage current is hard to flow, it is possible to provide a semiconductor device with high reliability or a high yield rate.

It is known that titnaium oxide takes two types of crystal structure, rutile and anatase, depending on its production method. For example, in Table 1 on page 385 of IMB Journal of Research and Development, Vol. 43, No. 3, it is shown that, as determined by CVD (chemical vapor deposition) method, titanium oxide takes the anatase phase at deposition temperature of 465°C or below, an anatase and rutile mixed structure at 550°C and 620°C, and the rutile phase at 660°C or above. It is also disclosed that

rutile type. Thus, use of rutile type titanium oxide for the conventional gate insulators is proposed because of better thermal stability of rutile type titanium oxide than that of anatase type.

In the conventional semiconductor devices, however, if it is tried to satisfy both requirements for high speed and low power consumption, tensile

strain is produced in the channel layer, and further, it is necessary to take a structure in which rutile type titanium oxide is used for the gate insulator. In such a structure, since the channel layer is placed under tensile strain, the leakage current flowing in the gate insulators increases, consequently causing a hike of power consumption.

Studies on this matter by the present inventors led to the elucidation of the mechanism of increasing the density of leakage current flowing in the rutile type titanium oxide gate insulators as a result of impartation of tensile strain to the channel layer. That is, according to the disclosed mechanism, as tensile strain is given to the channel layer, there is also produced tensile strain in the rutile type titanium oxide gate insulators, causing a decrease of the bandgap of the rutile type titanium oxide film while raising the tunneling probability, resulting in increased leakage current.

So, the present invention further provides a

semiconductor device incorporates MOS transistors having titanium oxide gate insulators interposed between the semiconductor substrate and gate electrodes, wherein the main crystal structure of said titanium oxide is anatase type, and tensile strain is given to the channel region of said semiconductor substrate.

By adopting anatase type for the main crystal structure of the titanium oxide gate insulators, it is possible to make the gate insulator bandgap greater than when rutile type is used. Also, even if tensile strain is exerted to the gate insulators, since the bandgap in the antase type is greater than that in the rutile type, it is possible to prevent the rise of tunneling current which would be caused by tensile strain, allowing a reduction of leakage current and realizing high-speed and low-power-consumption drive of the semiconductor device.

In the above embodiments, preferably a silicon oxide film or a titanium silicate film is disposed between the semiconductor substrate and the titanium oxide gate insulator.

Also, in either of the above embodiments, preferably the gate electrodes have a phosphorus- or boron-incorporated polycrystalline silicone film, and a silicon oxide or titanium silicate film is placed between the gate electrodes and the titanium oxide gate insulators.

Further, in either of the above embodiments, preferably the gate electrodes comprise a tungsten film, molybdenum film, tungsten nitride film, tungsten boride film, tungsten silicide film or a laminate thereof.

Still further, in either of the above embodiments, preferably the gate electrodes comprise a

ruthenium oxide film which is in contact with the said titanium oxide insulating film.

In the MOS transistors mentioned above, the electrodes may not necessarily be made of metals; they may be made of polycrystalline silicon or other suitable material. These MOS transistors can be used similarly to the conventional field effect transistors.

Now, the embodiments of the present invention are described in detail with reference to FIGS. 1 to 14 of the accompanying drawings.

Example 1

FIG. 1 is a schematic sectional view showing the structure of the principal part of the semiconductor device according to the first embodiment (Example 1) of the present invention, which view was taken along the line A-A' of FIG. 2 which shows a planar layout of the device. In the semiconductor device in this embodiment, as illustrated in FIG. 1, an element separating film 102 made of, for example, silicon oxide is provided on the surface of a P-type silicon substrate 101 to form an element forming region or domain 103. N-channel MOS transistors are provided in said element forming region 103.

Each MOS transistor has a gate insulator 104a and a gate electrode 105a and is flanked by a side wall 106a made of, for instance, silicon nitride. Gate insulator 104a is mainly composed of titanium oxide having a rutile type crystal structure, and gate

electrode 105a comprises, for example, a polycrystalline silicon film, a thin metal film, a metal silicide film or a laminate thereof.

Each MOS transistor also has an N^- type source/drain diffusion layer 107a formed as self-aligned to the gate electrode 105 and an N^+ type source/drain diffusion layer 108 formed as self-aligned to the element separating layer 102 and gate electrode 105a.

On the surface of this semiconductor device is provided a layer insulating film 109 in which are formed contact holes 110 which reach the N^+ type source/drain diffusion layer 108.

Supposing that the thickness of the rutile type titanium oxide gate insulator is 30 nm and the permittivities of rutile type titanium oxide and silicon oxide are 60 and 4.0, respectively, then the silicon oxide reduced thickness of the insulator is 2 nm, provided that they have the same dielectric properties. That is, the said rutile type titanium oxide gate insulator has a [illegible] and a reduced thickness of 2 nm.

The state of strain of the said gate insulator 104a made of titanium oxide is compressive.

Thus, in the semiconductor device of the present invention, since the gate insulator 104a is composed of rutile type titanium oxide which is a high-permittivity material, it is possible to make the

physical thickness of said insulators greater than when silicon oxide is used, thereby preventing DT current from flowing.

The bandgap of the gate insulator becomes greater than when no strain exists or when tensile strain is formed. The enlarged bandgap reduces the probability of electrons to pass through the insulator, thus holding back the rise of leakage current. Also, because of use of rutile type titanium oxide, there can be obtained a gate insulator which is thermally more stable than when anatase type titanium oxide is used.

Further, as shown in FIG. 3, a single layer or more layers of insulator 111 made of silicon oxide, silicon nitride, silicon oxide nitride or the like may be formed between the silicon substrate 101 and the gate insulator 104a. In this case, however, the thickness of such an insulator is preferably not greater than 0.5 nm for obtaining high permittivity of the gate insulator.

The gate electrode may be formed in two or more layers (e.g. [illegible]

The foregoing explanation concerns the embodiments where titanium oxide was used for the gate insulators, but the similar effect can be obtained by using zirconium oxide or hafnium oxide.

FIG. 5 depicts strain dependence of the bandgap of rutile type titanium oxide. Here, positive strain represents tensile strain and negative strain

represents compressive strain. It is seen from FIG. 5 that the bandgap of rutile type titanium oxide decreases with rise of tensile strain while increases with rise of compressive strain.

Strain dependence of the bandgap shown in FIG. 5 was determined from the first-principles band calculations. This first-principles band calculations are a method in which, as explained for instance in Iwanami Koza Modern Physics 7 "Solids - Structure and Physical Properties" (Iwanami Shoten, 1994), the Schrödinger's equation relating to the electrons in a solid is solved and the energy band of the electrons is calculated.

The "bandgap" is the energy difference between the upper edge of the energy level (valence electron band) occupied by the electrons and the lower edge of the energy level (conduction band) not occupied by the electrons. The greater the bandgap, the higher becomes the permittivity, hence the more restrained is the current flow. According to the density functional theory, the calculated [illegible] underestimated in comparison with the experimental values. In our calculations, therefore, the calculated values of bandgap were corrected according to the experimental results.

FIG. 6 shows strain dependence of the barrier height of rutile type titanium oxide. Here, positive strain represents tensile strain and negative strain

represents compressive strain. Assuming that the barrier height Φ_B (ε) is proportional to the bandgap Eg (ε) shown in FIG. 5, it was calculated from the following equation (1):

$$\Phi_B^R(\varepsilon) = \Phi_B^R(\varepsilon = 0) \times Eg(\varepsilon)/Eg(\varepsilon = 0) \quad (1)$$

Φ_B^R (ε = 0) is the barrier height when there exists no strain (ε), and it was here supposed to be 1.0 eV. The obtained value is the barrier height of rutile type titanium oxide of the bulk which has been obtained in the experiment.

It is seen from FIG. 6 that the barrier height of rutile type titanium oxide decreases with the rise of tensile strain but increases with the rise of compressive strain.

It is preferable to use the following equation (1') in place of the equation (1) for making calculations with higher precision.

$$\Phi_B^R(\varepsilon) = 1/2\,(E_g^R(\varepsilon) - E_g^{Si}) \quad (1')$$

E_g^{Si} : bandgap of silicon, ...

FIG. 7 depicts strain dependence of the leakage current of rutile type titanium oxide. (Silicon dioxide reduced thickness of rutile type titanium oxide = 2.0 nm; applied voltage = 1 V). Strain dependence of the leakage current density shown in FIG. 7 was determined from the relation between the probability of

the electrons to tunnel the insulating film and the strain by using the WKB approximation, as explained in, for instance, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 46, No. 2, page 354, by referring to strain dependence of the barrier height depicted in FIG. 6. The result shown in FIG. 7 is the one obtained when the applied voltage was 1 V and the silicon oxide reduced film thickness was 2 nm. The silicon oxide reduced thickness on the horizontal axis in FIG. 7 is the film thickness with which the same dielectric properties as silicon oxide can be obtained, and when it is assumed that the permittivities of silicon oxide and rutile type titanium oxide are 4.0 and 60, respectively, the thickness of the titanium oxide film whose silicon oxide reduced thickness is 2.0 nm comes to 2.0 nm × 60/4.0 = 30.0 nm. It can be learned from FIG. 7 that the leakage current density in rutile type titanium oxide rises with the increase of tensile strain and drops with the increase of compressive strain.

Example 2

For the explanation of the second embodiment of the present invention, reference is made to FIGS. 8 and 9 which show strain dependence of the bandgap of hafnium oxide. It is noted from FIGS. 8 and 9 that the bandgap of either of zirconium oxide and hafnium oxide decreases with the increase of tensile strain and increases with the increase of compressive strain. It

is recognized from this that the leakage current density in the case of zirconium oxide or hafnium oxide, as in the case of rutile type titanium oxide described above, rises with the increase of tensile strain and drops with the increase of compressive strain.

Example 3

The third embodiment of the present invention is described with reference to FIGS. 10, 11 and 12. FIG. 10 illustrates the structure in which the gate insulator is brought into a state of being compression strained, by for instance giving tensile strain to the gate electrode. When tensile strain is exerted to the gate electrode, its reaction brings the gate insulator into a state of being compression strained.

FIGS. 11 and 12 show a process for producing a semiconductor device having the tensile strained gate electrodes shown in FIG. 10 and the compression [illegible] titanium oxide gate insulators. First, 200 to 300 nm deep grooves are formed in the [illegible] type silicon substrate 101, and a silicon oxide film is embedded therein to form shallow-groove element separating layers 102 (FIG. 11A). Then, an approximately 30 nm thick rutile type titanium oxide film 104 is formed, by CVD for instance, on the surface of said silicon substrate 101 (FIG. 11B). In this operation, the film forming temperature is preferably

set to be not lower than 660°C. If the film forming temperature is below 660°C, anatase type titanium oxide may be allowed to exist in the titanium oxide film 104 and it may be phase shifted into rutile type in the ensuing heat treatment. Phase shift of titanium oxide from anatase to rutile type is attended by a volume shrinkage, which may give rise to tensile strain in the titanium oxide film 104.

Next, an amorphous silicon film 95 containing impurity phosphorus (P) is formed on the surface of the rutile type titanium oxide film 104 by CVD. The thickness of this amorphous silicon film 95 is made about 200 nm for instance (FIG. 11C).

Further, the semiconductor substrate temperature is raised to 600°C or above to crystallize the amorphous silicon film 95 to form a polycrystalline silicon film 105. Since crystallization of amorphous silicon is attended by volume shrinkage, the polycrystalline silicon film 105 formed by the [illegible] brought into a tensile strained state, and by the reaction of this tensile [illegible] rutile type titanium oxide film 104 is turned into a compression strained state. Crystallization of the amorphous silicon film 95 may be effected by controlling the semiconductor substrate temperature, but laser irradiation may be employed (FIG. 11D).

Then, using a photoresist film as a mask, the polycrystalline silicon film 105 and rutile type

titanium oxide film 104 are etched to form the gate insulators 104a and gate electrodes 105a of the MOS transistors, after which an approximately 2 nm thick silicon oxide film 96 is formed by thermal oxidation or CVD. Then an N^- type source/drain domain 107 of the MOS transistors is formed by ion implantation of phosphorus (P). This N^- type source/drain domain 107 is formed as self aligned to the gate electrodes and gate insulators. The purpose of forming the said silicon oxide film 96 is to minimize the damage to the silicon substrate by ion implantation of phosphorus (P).

Then silicon nitride 106 is deposited on the semiconductor substrate surface to a thickness of 200 nm by sputtering or CVD (FIG. 12B) and the deposited silicon nitride film 106 and silicon oxide film 96 are etched to form side walls 106a of the gate electrodes and gate insulators (FIG. 12C).

Next, the element separating film 102, gate electrodes 106a and side walls 106a are masked and an N^+ source/drain diffusion layer 108 is formed by ion implantation of arsenic. Further, a [illegible] film 109 is formed by CVD, and in this insulating film are formed contact holes 110 which reach the surface of the diffusion layer.

Although the above-described production process concerns the case involving the N-channel MOS transistors, this process can be applied to the case where the P-channel MOS transistors are used. It can

also be applied to the case of using CMOS transistors or BiCMOS transistors.

The gate electrode 105 may comprise, besides the polycrystalline silicon film mentioned above, a thin film of a metal such as tungsten and molybdenum, a metal compound such as tungsten nitride, or a metal silicide such as tungsten silicide, or a laminate thereof. Since no depletion is produced in the gate electrode film made of a metal such as tungsten or molybdenum, it is possible to reduce the effective thickness of the gate insulator. Also, tungsten is thermally stable and scarcely causes a change in film quality in the high-temperature processing after formation of the electrode film. In case the films are laminated with titanium oxide and tungsten contacting each other, there may be formed tungsten oxide. Tungsten oxide has lower permittivity than titanium oxide, and formation of such tungsten oxide leads to an increase of the reduced thickness of the gate [illegible]. It is therefore effective to use a tungsten nitride or tungsten silicide film having [illegible] oxidation resistance than the tungsten film. Tungsten nitride especially excels in oxidation resistance. In case the tungsten nitride film is used for the gate electrode, it is advantageous to form a two-layer structure of gate electrode as shown in FIG. 4. By using tungsten nitride for the layer (105a in FIG. 4) contacting titanium oxide, and by composing the

overlying layer (112 in FIG. 4) with tungsten which is lower in resistance than tungsten nitride, it is possible to obtain a low-resistance gate electrode.

In case of using the above materials for the gate electrode film, the gate insulator is brought into a compression strained state by controlling the film forming conditions. For example, in the case of the above-mentioned metals and metal compounds, a tensile strained state is produced by depositing them by sputtering at a film forming temperature of 300°C, and when a film of these metals or metal compounds is used for the gate electrode, the rutile type titanium oxide gate insulator is brought into a compression strained state by the force of reaction. Thus, the rutile type titanium oxide gate insulator assumes a compression strained state.

As explained above, the gate insulator 104a made of titanium oxide takes a compression strained state, and the bandgap thereof becomes greater than [illegible] strain or is in a state of being tensile strained.

Also, since the gate insulator 104a is composed of rutile type titanium oxide which is a high-permittivity material, it is possible to increase the physical thickness of the insulator as compared with the case where silicon oxide is used for the insulator, and to thereby prevent the DT current from flowing.

Further, because of use of rutile type

titanium oxide for the gate insulator 104a, there can be obtained an insulator which is thermally more stable than when using anatase type titanium oxide for the gate insulator.

This makes it possible to lessen the probability of the electrons passing through the insulator, and to check the increase of leakage current.

Positive avoidance of the gate insulator 104a from being brought into a state of tensile strain is an expedient way for preventing increase of leakage current in the gate insulator 104a. For avoiding the gate insulator 104a from being turned into a tensile strained state, the crystal structure of titanium oxide used for the insulator is made rutile before formation of the insulating film. This is because according to the method in which titanium oxide of anatase type crystal structure is made into a film and then turned into rutile structure by phase transition, there may be produced a rutile structure retaining tensile strain. Since the density of anatase type [illegible] smaller than that of rutile type titanium oxide, anatase-to-rutile phase transition is attended by volume shrinkage, which involves the risk of generating tensile strain in the rutile type titanium oxide gate insulator.

A method for confirming the compression strained state of the titanium oxide gate insulator is

to determine the interatomic distance between the titanium (Ti) atom and the oxygen (O) atom in titanium oxide by a transmission electron microscope (TEM). When no strain exists, the interatomic distance is 0.196 nm on the average. This indicates that when the average value of the interatomic distance is greater than 0.196 nm, the rutile type titanium oxide film will be in a tensile strained state, and when the average value of said distance is less than 0.196 nm, then said film will be in a compression strained state.

Example 4

FIG. 13 is a schematic sectional view showing the structure of the principal part of the semiconductor device according to the fourth embodiment of the present invention, which view was taken along the line A-A' of FIG. 14 which shows a planar layout of the device.

The semiconductor device of the present invention has I/O circuits connected directly to the external devices and [illegible] be connected to the external devices. These I/O circuits and internal circuits comprise single-channel MOS transistors, C-MOS transistors or BiCMOS transistors. In this Example, for simplicity of the explanation, we merely refer to a semiconductor device which comprises only the N-channel MOS transistors having a source/drain diffusion layer of LDD structure.

In the semiconductor device of this embodiment, as shown in FIG. 13, an element separating film 102 made of, for example, silicon oxide is formed on the surface of a P-type silicon substrate 101. There are also provided an internal circuitry forming region 203 and an I/O circuitry forming region 303 in which the first N-channel MOS transistor and the second N-channel MOS transistor are formed respectively. The first MOS transistor formed in the internal circuitry forming region 203 has a gate insulator 204a and a gate electrode 205a. Gate electrode 205a is flanked by the side walls 206a which are made of, for example, silicon nitride. The main composing material of the gate insulator 204a is titanium oxide having a rutile type crystal structure. Gate electrode 205a comprises, for instance, a polycrystalline silicon film, a thin metal film, a metal silicide film, or a laminate thereof. In Fig. 13, the gate electrode 205a has a laminated structure, as one example.

The first MOS transistor has an N^- type source/drain diffusion [illegible] aligned to the gate electrode 205a and an N^+ type source/drain diffusion layer 208 self-aligned to the element separating layer 102 and gate electrode 205a.

When it is supposed that the thickness of said rutile type titanium oxide gate insulator is 30 nm and that the permittivities of rutile type titanium oxide and silicon oxide are 60 and 4.0, respectively,

then the silicon oxide reduced thickness of said insulator is 2 nm, provided that they have the same dielectric properties. That is, the physical thickness of said insulator is 30 nm and its reduced thickness is 2 nm. Therefore, as the gate insulator 204a is composed of rutile type titanium oxide which is a high-permittivity material, it is possible to increase the physical thickness of the gate insulator as compared with the case where silicon oxide is used for the gate insulator 204a, and to thereby prevent the DT current from flowing.

The second MOS transistor formed in the L/O circuitry forming region 303 has a gate insulator 304a and a gate electrode 305a which is flanked by the side walls 306a made of, for example, silicon nitride. The gate insulator 304a comprises a silicon oxide film which is, for instance, 5 nm thick, or a laminate of a silicon oxide film of for instance 3 nm thickness and a 30 nm thick rutile type titanium oxide film. Supposing that the permittivities of rutile type titanium oxide and silicon oxide are [illegible] silicon oxide reduced thickness of said laminate is 5 nm, provided that they have the same dielectric properties. Thus, the physical thickness of said insulator is 35 nm and its reduced thickness is 5 nm. As shown in Fig. 13, the gate electrode 305a has a laminated structure, as one example.

Each gate electrode 305a may comprise, for

example, a polycrystalline silicon film, a thin metal film, a metal silicide film, or a laminate thereof. The second MOS transistor has an N^- type source/drain diffusion layer 307a formed as self-aligned to the gate electrode 305a, and an N^+ type source/drain diffusion layer 308 formed as self-aligned to the element separating layer 102 and the gate electrode 305a.

In the above, the gate electrodes 205a and 305a have the laminated structure, but needless to say, these gate electrodes are not limited thereto and can take other structures.

A layer insulating film 109 is provided on the surface of this semiconductor device, and in this insulating film are formed contact holes 210, 310 which reach the N^+ type source/drain diffusion layers 208, 308, respectively.

In the first MOS transistor formed in the internal circuitry region, a high-permittivity film is used as the gate insulator like the MOS transistors shown in Example 1. Also, the gate length is shortened [illegible] suited for high-speed operation.

The MOS transistor for the I/O circuits is not so strongly required to have adaptability to high-speed operation as the MOS transistors of the internal circuits (e.g. circuits for calculation), and is rather required to be resistant to high voltage in the event of application of high voltage to the gate. Therefore,

the second MOS transistor formed in the I/O circuitry region has a silicon oxide gate insulator 304a having a thickness of 3 nm or greater. A silicon oxide film of 3 nm or greater thickness is useful for reducing both of DT current and FN current. Thus, the second MOS transistor is resistant to high voltage applied between the gate electrode and the substrate and highly reliable in use as a transistor for I/O circuits.

According to this embodiment of the present invention, the MOS transistors suited for high-speed operation as an internal circuit element and the MOS transistors showing high resistance to high voltages as an I/O circuit element are both provided on the same substrate, so that it is possible to provide a semiconductor device with high reliability and low production cost.

The gate insulator 204a made of titanium oxide is preferably in a compression strained state. This makes it possible to increase the gate insulator bandgap as compared with the case where no strain exists or the film is tensile.

Example 2, and consequently, it becomes possible to lessen the probability of the electrons being allowed to pass through the insulator, and to thereby check rise of leakage current.

A single or more layers of insulating film made of silicon oxide, silicon nitride, silicon oxide nitride or the like may be formed between the silicon

substrate 101 and the gate insulator 204a. The thickness of such an insulating film, however, is preferably not greater than 0.5 nm for securing high permittivity of the gate insulator.

Also, the gate electrodes 205a, 305a may be formed in two or more layers as shown in FIG. 4.

Thus, according to the present invention, the gate insulator made of rutile type titanium oxide is in a compression strained state, and its bandgap is greater than provided when no strain exists or when the insulator is tensile strained. This contributes to lessening the probability of the electrons to pass through the insulator, making it possible to check the increase of FN leakage current and to provide a titanium oxide gate insulator structure which checks the flow of leakage current. It also becomes possible to provide the semiconductor devices with high reliability in a high yield.

Example 5

The semiconductor device according to the fifth embodiment of the present invention and its production process are explained with reference to FIGS. 15 to 21.

First, the construction of the semiconductor device according to this embodiment is described by referring to FIGS. 15 and 16.

FIG. 15 is a schematic sectional view

showing, in section, the structure of the principal part of the semiconductor device according to Example 5 of the present invention, which view was taken along the line A-A' of FIG. 16 which shows a planer layout of the principal part of the semiconductor device of the instant embodiment.

In the semiconductor device according to this Example, as shown in FIG. 15, an element separating film 102 made of, for example, silicon oxide and an element forming region 103 are formed on the surface of a P-type silicon substrate 101, and N-channel MOS transistors are provided in said element forming region 103.

Each MOS transistor has a gate insulator 104a and a gate electrode 105a flanked by the side walls 106a made of, for example, silicon nitride. Said gate insulator 104a is mainly composed of titanium oxide having an anatase type crystal structure. The gate electrode 105a comprises, for instance, a polycrystalline silicon film, a thin metal film, a metal silicide [illegible]

The MOS transistor has an N^- type source/drain diffusion layer 107a formed as self-aligned to the gate electrode 105a and an N^+ type source/drain diffusion layer 108 formed as self-aligned to both of the element separating layer 102 and the gate electrode 105a.

A film 20 having tensile stress is formed on the surface of the MOS transistor. This tensile

stressed film 20 is made of, for instance, silicon nitride. By this film 20, the channel region 10 of the silicon substrate is brought into a tensile strained state to lessen the effective mass of the carrier and realize speed-up of the device. The tensile stressed film 20 also produces tensile strain in the gate insulator.

A layer insulating film 109 is formed on the surface of this semiconductor device, and in said insulating film 109 are provided contact holes 110 which reach the N^+ type source/drain diffusion layer 108.

The thickness of the anatase type titanium oxide gate insulator 104a is, for instance, 30 nm. Assuming that the permittivities of anatase type titanium oxide and silicon oxide are 60 and 4.0, respectively, then the silicon oxide reduced thickness of the gate insulator 104a is 2 nm, provided that they have the same dielectric properties. Namely, the physical thickness of the insulator is 30 nm and its reduced thickness is 2 nm.

Thus, in the semiconductor device according to the instant embodiment of the present invention, the gate insulator 104a is composed of anatase type titanium oxide which is a high-permittivity material, so that it is possible to increase the physical thickness of the gate insulator 104a as compared with

the case where the insulator is made of silicon oxide, and to thereby prevent the DT current from flowing.

Also, since titanium oxide whose main crystal structure is anatase type is used for the gate insulator, it is possible to make the insulator bandgap greater than provided when using rutile type titanium oxide. Further, even if tensile strain is given to the gate insulator, the anatase type bandgap is greater than the rutile type bandgap, so that it is possible to inhibit the rise of tunneling current due to tensile strain.

Here, tensile strain dependence of anatase type titanium oxide used for the semiconductor device in the instant embodiment of the present invention is discussed in comparison with the properties of rutile type titanium oxide by referring to FIGS. 17 to 19.

First, tensile strain dependence of the bandgap of titanium oxide is explained with reference to FIG. 17.

FIG. 17 is a graphic illustration of tensile strain dependence of [illegible]

the graph, tensile strain ε (%) is plotted as abscissa and bandgap Eg (eV) as ordinate. Solid line A represents anatase type and solid line B represents rutile type.

As will be understood from FIG. 17, both of the bandgap Eg^R (ε) of rutile type titanium oxide R and the bandgap Eg^A of anatase type titanium oxide A

decrease as strain is accumulated, but $Eg^A(\varepsilon)$ never becomes smaller than $Eg^R(\varepsilon)$.

Next, tensile strain dependence of barrier height of titanium oxide is explained with reference to FIG. 18.

FIG. 18 is a graphic illustration of tensile strain dependence of barrier height of titanium oxide. In the graph, tensile strain ε (%) is plotted as abscissa and barrier height Φ_B (eV) as ordinate. Positive strain indicates tensile strain and negative strain indicates compressive strain. Solid line A represents anatase type and solid line B represents rutile type.

Here, it was assumed that barrier height $\Phi_B^R(\varepsilon)$ was proportional to the bandgap Eg shown in FIG. 17, and barrier height of rutile type $\Phi_B^R(\varepsilon)$ was calculated from the following equation (1) while barrier height of anatase type $\Phi_B^A(\varepsilon)$ was calculated from the following equation (2).

$$\Phi_B^A(\varepsilon) = \Phi_B^A(\varepsilon = 0) \times Eg^A(\varepsilon)/Eg^R(\varepsilon = 0) \qquad (2)$$

Here, $\Phi_B^R(\varepsilon = 0)$ is barrier height of rutile type when there existed no strain ($\varepsilon = 0$), and it was supposed that $\Phi_B^R(\varepsilon = 0) = 1.0$ eV. This value is barrier height of rutile type titanium oxide of the bulk obtained in the experiment.

It is desirable for making the calculations with higher precision to use the following equations (1') and (2') in place of the above-shown equations (1) and (2).

$$\Phi_B^R(\varepsilon) = 1/2\,(E_g^R(\varepsilon) - E_g^{Si}) \qquad (1')$$

$$\Phi_B^A(\varepsilon) = 1/2\,(E_g^A(\varepsilon) - E_g^{Si}) \qquad (2')$$

wherein E_g^{Si} is bandgap of silicon and = 1.1 eV.

As is seen from FIG. 18, barrier height of rutile type titanium oxide, $\Phi_B^R(\varepsilon)$, and barrier height of anatase type titanium oxide, $\Phi_B^A(\varepsilon)$, decrease as strain is accumulated, but $\Phi_B^R(\varepsilon)$ never becomes smaller than $\Phi_B^A(\varepsilon)$.

Next, tensile strain dependence of the leakage current density of titanium oxide is explained with reference to FIG. 19.

FIG. 19 is a graphic illustration of tensile strain dependence of the leakage current density of barrier height of titanium oxide. In the graph, tensile strain ε (%) is plotted as abscissa and current density (A/cm^2) as ordinate. Positive strain indicates tensile strain and negative strain indicates compressive strain. Solid line A represents anatase type and solid line R represents rutile type.

FIG. 19 shows the result when the applied voltage was 1 V and the silicon oxide equivalent thickness of the film was 2.0 nm. The silicon oxide

equivalent thickness on the horizontal axis in FIG. 5 is the film thickness at which the same dielectric properties as silicon oxide can be obtained. When it is assumed that the permittivities of silicon oxide and rutile type titanium oxide are 4.0 and 60, respectively, then the titanium oxide film thickness whose silicon oxide equivalent thickness is 2.0 nm becomes 2.0 nm × 60/4 = 30.0 nm.

It is seen from FIG. 19 that the leakage current densities of rutile type titanium oxide and anatase type titanium oxide rise up monotonously as the strain increases, but even if the strain is exerted, the leakage current density of anatase type titanium oxide remains smaller than that of rutile type titanium oxide. Thus, even if tensile strain is applied to the gate insulator as a result of impartation of tensile strain to the channel layer, it is possible to inhibit the rise of leakage current as compared with the case where rutile type is used, by using anatase type titanium oxide for the gate insulator. This leads to a reduction of power [illegible].

A method of producing the semiconductor device according to the instant Example is described with reference to FIGS. 20A to 20F which are a flow chart showing a process for producing the semiconductor device according to Example 5 of the present invention.

First, as shown in FIG. 20A, 200 to 300 nm deep grooves are formed in the surface of a P-type

silicon substrate 101, and silicon oxide films are embedded therein to form shallow-groove element separating layers 102.

Next, as shown in FIG. 20B, an approximately 30 nm thick anatase type titanium oxide film 104 is formed on the surface of the silicon substrate 101 by CVD or other suitable method. In this operation, the film forming temperature should be not higher than 460°C, preferably not higher than 330°C. If the film forming temperature is over 460°C, there is a possibility that rutile type titanium oxide be mingled in the titanium oxide film 104 when it is formed. If the film forming temperature is below 330°C, it is likely that anatase to rutile phase transition would take place in the ensuing heat treatment at around 850°C. An N^+ type polycrystalline silicon film 105 with a thickness of about 200 nm is formed on the surface of the anatase type titanium oxide film 104 by CVD or other suitable means.

Then, as shown in FIG. 20C, the polycrystalline silicon film and titanium oxide film 104 are etched through photoresist masking to form gate insulators 104a and gate electrodes 105a of the MOS transistors. This is followed by formation of an approximately 2 nm thick silicon oxide film 96 by thermal oxidation or CVD. An N^- type source/drain region 107 of MOS transistor is formed by ion implantation of phosphorus. This N^- type

source/drain region 107 is designed as self-aligned to the gate electrodes and gate insulators. The purpose of forming the silicon oxide film 96 is to lessen the damage to the silicon substrate by ion implantation of phosphorus.

Then, as shown in FIG. 20D, a 200 nm thick silicon nitride film 106 is formed on the surface of the semiconductor substrate by sputtering or CVD.

Further, as illustrated in FIG. 20E, the silicon nitride film 106 and silicon oxide film 96 are etched to form the side walls 106a flanking the gate electrodes and gate insulators.

Finally, as shown in FIG. 20F, an N^+ type source/drain diffusion layer 108 is formed by ion implantation of arsenic through masking of element separating film 102, gate electrodes 105a and side walls 106a. Further, a 200 nm thick silicon nitride film 20 is deposited on the semiconductor substrate surface by CVD. This silicon nitride film formed by [illegible] produces a tensile stress, whereby the channel section 10 of the silicon substrate and the [illegible] insulator 104a are also pulled and brought into a tensilely strained state. A layer insulating film 109 is formed by CVD, and in this insulating film are formed contact holes 110 which reach the surface of the diffusion layer. This completes formation of the principal part of the semiconductor device according to the instant embodiment shown in FIG. 15.

The above-described production process concerns adaptation of the N-channel MOS transistors, but this process can also be applied to the structures involving the P-channel MOS transistors, CMOS transistors or BiCMOS transistors.

The gate electrode 105a may comprise, besides a polycrystalline silicon film mentioned above, a thin film of a metal such as tungsten and molybdenum or a metal compound such as tungsten nitride and tungsten boride, a film of a metal silicide such as tungsten silicide, a luthenium oxide film, or a laminate thereof. Use of these materials is conducive to the reduction of resistance of the gate electrodes. In a structure where a ruthenium oxide film and a tungsten oxide insulating film are placed in contract with each other, an improvement of thermal stability of the titanium oxide gate insulator can be expected.

Since anatase type titanium oxide is thermally unstable in comparison with rutile type as mentioned above, there may take place anatase-to-rutile phase transition in annealing after film formation. However, in this embodiment of the present invention which features anatase type main crystal structure of the titanium oxide gate insulator, even if the film contains several to around 10% of rutile type, such matter scarcely affects the effect of the instant embodiment of the invention and falls within the range of concept of the present invention.

As explained above, in the semiconductor device according to the present Example, since the channel region of the silicon substrate is in a tensilely strained state, the effective mass of the carrier electrons is reduced and a high-speed semiconductor device is realized.

Further, in this Example of the invention, since the main crystal structure of the titanium oxide gate insulator is anatase type, it is possible to make the bandgap of the gate insulator greater than available with the rutile type. Also, even if tensile strain is exerted to the gate insulator, the anatase type bandgap can be made greater than the rutile type bandgap. This makes it possible to check the rise of tunneling current due to tensile strain and to thereby lessen power consumption of the device.

Accordingly, reliability of the semiconductor device is enhanced and, as a result, its yield is elevated.

Example 6

The structure of the semiconductor device according to the sixth embodiment of the present invention is explained with reference to FIG. 21.

FIG. 21 is a schematic sectional view showing the structure of the principal part of the semiconductor device according to Example 6 of the present invention. The reference numerals used in the

drawing correspond to those in FIG. 15.

In this embodiment, as shown in FIG. 21, an insulating film made of, for instance, silicon oxide, silicon nitride or silicon oxide nitride, or a titanium silicate film 111 is formed in single or more layers between the silicon substrate 101 and the titanium oxide gate insulator 104a. The thickness of such an insulating film 111 is preferably not greater than 0.5 nm for providing the desired dielectric properties of the gate insulator. The presence of said film between the silicon substrate 101 and the titanium oxide gate insulator is conducive to the improvement of thermal stability of the titanium oxide gate insulator.

It is possible with this embodiment, too, to realize speed-up and a reduction of power consumption of the semiconductor device. It is also possible to enhance reliability of the device and, consequently, to raise the yield.

The structure of the semiconductor device according to the seventh embodiment of the present invention is described with reference to FIG. 22.

FIG. 22 is a schematic sectional view showing the structure of the principal part of the semiconductor device according to Example 7 of the present invention. The reference numerals in the drawing correspond to those used in FIG. 15.

In this embodiment, as shown in the drawing, the gate electrode is composed of the films 105a and 112 in two or more layers. The film 112 may be made of a silicide, the same material as used for the film 105a, aluminum (Al), tungsten (W) or the like.

This embodiment, too, is capable of realizing speed-up and a reduction of power consumption of the semiconductor device. Accordingly, reliability of the semiconductor device is enhanced and its yield is raised.

It will be further understood by those skilled in the art that the foregoing description has been made on embodiments of the invention and that various changes and modifications may be made in the invention without departing from the spirit of the invention and the scope of the appended claims.